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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,690	07/28/2003	Etsuro Morita	JG-SU-5004C/500577.20052	6077

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REED SMITH, LLP
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EXAMINER	
SONG, MATTHEW J	
ART UNIT	**PAPER NUMBER**
1722	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,690	MORITA ET AL.	
	Examiner	Art Unit	
	Matthew J. Song	1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6 and 23-32* is/are pending in the application.

4a) Of the above claim(s) *23-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 6 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 6 recites, " V/Ga and V/Gb become 0.23 to 0.50 mm^2/minute °C, respectively, both V/Ga and V/Gb exceeding a first critical ratio $((V/G)_1$ for restricting vacancy agglomerates to a vacancy point defect dominant domain at the center of the ingot, such that no OSF rings are caused in the ingot" in lines 8-12. The instant specification does not provide support for no OSF rings. The specification merely teaches V/Ga and V/Gb lower than 0.23 mm^2/minute °C leads to a problem of occurrence of OSF's, note page 30, lines 1-5 of the specification. There is no explicit teaching that no OSF ring will be formed.

3. Claim 6 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 6 recites, " V/Ga and V/Gb

become 0.23 to 0.50 mm^2/minute °C, respectively, both V/Ga and V/Gb exceeding a first critical ratio $((V/G)_1$ for restricting vacancy agglomerates to a vacancy point defect dominant domain at the center of the ingot, such that no OSF rings are caused in the ingot" in lines 8-12. The claim in not enabled to produce a wafer with no OSF ring at 0.23 mm^2/minute. Yokoyama et al teaches an OSF ring is formed with a radius of 77.0 mm at a V/G ratio of 0.233 mm^2/°C minute and a OSF ring is formed with a radius of 90.0 mm at a V/G ratio of 0.250 mm^2/°C minute, note Table 1. Based on applicant's claim a wafer with no OSF is necessarily formed at 0.23 mm^2/°C minute, which is directly contradicted by Yokoyama's teaching. The claim is not enabled over the entire claimed range.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abe et al (EP 0926718 A2) in view of Hourai et al (US 5,954,873) or Yokoyama et al (US 6,179,910).

Abe et al discloses a method of heat treating a silicon monocrystalline wafer at 1200°C or above for 30 minutes or more in a reducing atmosphere of 100% hydrogen or a mixed atmosphere of hydrogen and argon to decrease the crystal originated particle (COP) density to zero ([0044]). Abe et al also discloses growing a silicon monocrystal ingot by the Czochralski method, this reads on applicants' pulling a single crystal ingot from a silicon melt, and obtaining a wafer by slicing the ingot ([0016]). Abe et al also discloses growing the silicon ingot at a growth rate greater than 0.6 mm/min, such that one void COPs exist in a high density (claims 2-7). Abe et al also discloses a single type defect in light scattering tomography defect (LSTD) in a rapidly cooled CZ crystal with COPs existing in a silicon monocrystal subjected to the heat treatment preferably have a size of 60-130 nm (0.06-0.13 μm) ([0022] and [0034]-[0036]) and the number of COPs was 90 per 8 inch wafer ([0068]), which can be determined to be approximately 0.069 pieces/cm^2. Abe et al also teaches COP is one type of crystal defect that is introduced in a crystal during growth and is known to be a vacancy type defect having a void structure ([0005]) and pulling at a growth rate of 0.6 mm/min, so COPs exist in a high density (Abstract).

Abe et al does not teach pulling up the ingot such that V/Ga and V/Gb become 0.23-0.50 mm^2/minute °C, respectively, both of V/Ga and V/Gb exceeding a first critical ratio for restricting vacancy agglomerates to a vacancy point defect dominant domain at the center of the ingot.

In a method of manufacturing a silicon single crystal, Hourai et al teaches the V/G value effects the density and distribution of all types of defects in the crystal, where V is the pulling rate (mm/min) and G is the inside-crystal gradient in the direction of the pulling axis in a high temperature zone from the melting point of silicon to 1300°C (col 4, ln 30-67). Hourai et al also teaches an infrared scattering defect developing region is obtained at V/G ratios of greater than approximately 0.23 mm^2/°C minute (Fig 2 and col 3, ln 15-25).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Abe et al by using the V/G for the center and edge taught by Hourai et al to produce a crystal containing the light scattering defects desired by Abe et al and with no OSF ring because Abe et al only desires COP defects.

The combination of Abe et al and Hourai et al teach heat treating at a temperature of 1200°C or above for 30 minutes or more ('718 Abstract), which overlap the claimed range of 1050-1220°C for 30-150 minutes. Overlapping ranges are held to be obvious (MPEP 2144.05).

The combination of Abe et al and Hourai et al teach pulling a single crystal ingot under the claimed pulling conditions and heat treating in a similar method, as claimed by applicants. The combination of Abe et al and Hourai et al also teach the heat treatment decrease the density of COPs and the number of COPs with a size of 0.2-0.12 μm is 0.069 pieces/cm^2. The combination of Abe et al and Hourai et al is silent to the number of COPs with a size less than 0.12 μm. However, since the combination of Abe et al and Hourai et al teach pulling a crystal and heat treating a wafer, as claimed by applicants, and the heat treatment is known to reduce COPs; the claimed number of COPs smaller than 0.12 μm is inherent to the combination of Abe et al and Hourai et al.

In a method of manufacturing silicon, Yokoyama et al teaches a V/G ratio greater than 0.25 $mm^2/°C$ min produces a silicon ingot with only a void effect region (Fig 2). Yokoyama et al also teaches pulling under a condition of V/G values smaller than 0.25 $mm^2/°C$ to miniaturize the sizes of void defects and the wafers are heat treated by hydrogen gas so as to eliminate void defects (col 3, ln 1-41). Yokoyama et al also teaches G is measured at a temperature near the melting point at sites along its crystal axis, this reads on applicants' center and edge because Yokoyama et al teaches points along the axis which includes the center and edge of the ingot (col 3, ln 35-45). Yokoyama et al also teaches manufacturing crystals with a V/G value smaller than 0.3 $mm^2/°C$ min suitable for hydrogen heat treatment (col 9, ln 50 to col 10, ln 45). Yokoyama et al also teaches a hydrogen heat treatment of 1200°C for 1 hour (col 6, ln 20-55), this reads on applicants' heat treatment of a 100% hydrogen atmosphere at a temperature of 1050-1220°C for 30-150 minutes. Yokoyama et al teaches wafers cut from a silicon single crystal (col 4, ln 10-25). Yokoyama et al also teaches no OSF ring is present at a V/G greater than 0.25 $mm^2/°C$ minute, note Fig 2. Yokoyama et al also teaches V/G ratios and defects size, particularly a V/G ratio of 0.38 mm^2/minute °C producing a defect size of 51.8-164.7 nm (Table 2).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Abe et al by pulling with a V/G greater than 0.25 $mm^2/°C$ minute, as taught by Yokoyama et al, to form a wafer without an OSF ring and with a high density and size of void defects, which is desired by Abe et al.

The combination of Abe et al and Hourai et al teach pulling a single crystal ingot under the claimed pulling conditions and heat treating in a similar method, as claimed by applicants. The combination of Abe et al and Hourai et al also teach the heat treatment decreases the number

of defects. The combination of Abe et al and Hourai et al is silent to the claimed number of COPs resulting from the heat treatment. However, since the combination of Abe et al and Hourai et al teaches a similar method of pulling a crystal and heat treating a wafer, as claimed by applicants, the claimed number of COPs is inherent to Yokoyama et al.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claim 6 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 of U.S. Patent No. 6,547,875 in view of Abe et al (EP 0926718 A2).

US 6,574,875 ('875) claims a method of pulling a silicon single crystal ingot with a V/Ga and V/Gb of 0.23 to 0.50 mm^2/minute °C, where the temperature gradient is in a temperature range from the melting point of silicon to 1300°C. The wafer inherently does not have an OSF ring because '875 claims the same process parameters used by applicant's to produce a wafer with no OSF ring.

'875 does not claim the heat treatment of silicon wafer.

Abe et al discloses a method of heat treating a silicon monocrystalline wafer at 1200°C or above for 30 minutes or more in a reducing atmosphere of 100% hydrogen or a mixed atmosphere of hydrogen and argon to decrease the crystal originated particle (COP) density to zero ([0044]). Abe et al also discloses growing a silicon monocrystal ingot by the Czochralski method, this reads on applicants' pulling a single crystal ingot from a silicon melt, and obtaining a wafer by slicing the ingot ([0016]). Abe et al also discloses growing the silicon ingot at a growth rate greater than 0.6 mm/min, such that one void COPs exist in a high density (claims 2-7). Abe et al also discloses a single type defect in light scattering tomography defect (LSTD) in a rapidly cooled CZ crystal with COPs existing in a silicon monocrystal subjected to the heat treatment preferably have a size of 60-130 nm (0.06-0.13 μm) ([0022] and [0034]-[0036]) and the number of COPs was 90 per 8 inch wafer ([0068]), which can be determined to be approximately 0.069 pieces/cm^2. Abe et al also teaches COP is one type of crystal defect that is introduced in a crystal during growth and is known to be a vacancy type defect having a void structure ([0005]) and pulling at a growth rate of 0.6 mm/min, so COPs exist in a high density (Abstract).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the silicon wafer of '875 by performing the heat treatment taught by Abe et al to produce a defect free wafer.

The combination of '875 and Abe et al does not teach the number of resulting COP, but this would be inherent since the combination of '875 and Abe et al teach a similar method, as applicant, and a similar method is expected to produce similar results.

Response to Arguments

5. Applicant's arguments with respect to claim 6 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's arguments filed 6/22/2005 have been fully considered but they are not persuasive.

Applicant's argument that Hourai et al and Yokoyama teach forming an OSF ring is noted but is not found persuasive. While Hourai et al and Yokoyama et al teach forming a silicon ingot, which contains an OSF ring; Hourai et al and Yokoyama are not limited to those teachings. Abe et al, the primary reference, teaches pulling a silicon single crystal at a high pulling rate of greater than 0.6 mm/min to form a large number of COPs, which can be eliminated with a heat treatment to from a silicon monocrystal wafer with no defects (Abstract). Abe et al does not teach the claimed V/G ratio, however Abe et al's teaching suggests the claimed ratio would be desirable since Abe et al teaches using a high pulling rate, V, which would result in a large V/G ratio. Hourai et al and Yokoyama et al both teach the effects of V/G on the defect distribution of a silicon single crystal and both teach the V/G ratio affects the type and position of defects, note Fig 2 of Yokoyama and Fig 2 of Hourai. Hourai et al and Yokoyama et al teach the V/G ratios necessary to produce a silicon single crystal with no OSF and a high density of COPs, which is desired by Abe et al. Abe et al only teaches controlling V, however in view of Hourai et al and Yokoyama et al, the effect of G also requires control to produce a silicon single crystal ingot with COPs and no OSF ring.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Park et al (US 6,472,040) teaches critical V/G ratios for controlling defect distribution (col 9, ln 30-65).

Fusegawa et al (US 5,834,322) teaches pulling a silicon single crystal at a speed not less than 0.8 mm/min, slicing wafers from the ingot and heat treating the wafers in a temperature range of 1150-1280°C for 10-120 minutes to eliminate defects (col 3, ln 1-67).

Falster et al (US 2003/0051657) teaches controlling V/G to form vacancy dominated silicon single crystals ([0044]-[0047] and Abstract).

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J. Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Duane Smith can be reached on 571-272-1166. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song
Examiner
Art Unit 1722

MJS
September 9, 2005

ROBERT KUNEMUND
PRIMARY EXAMINER